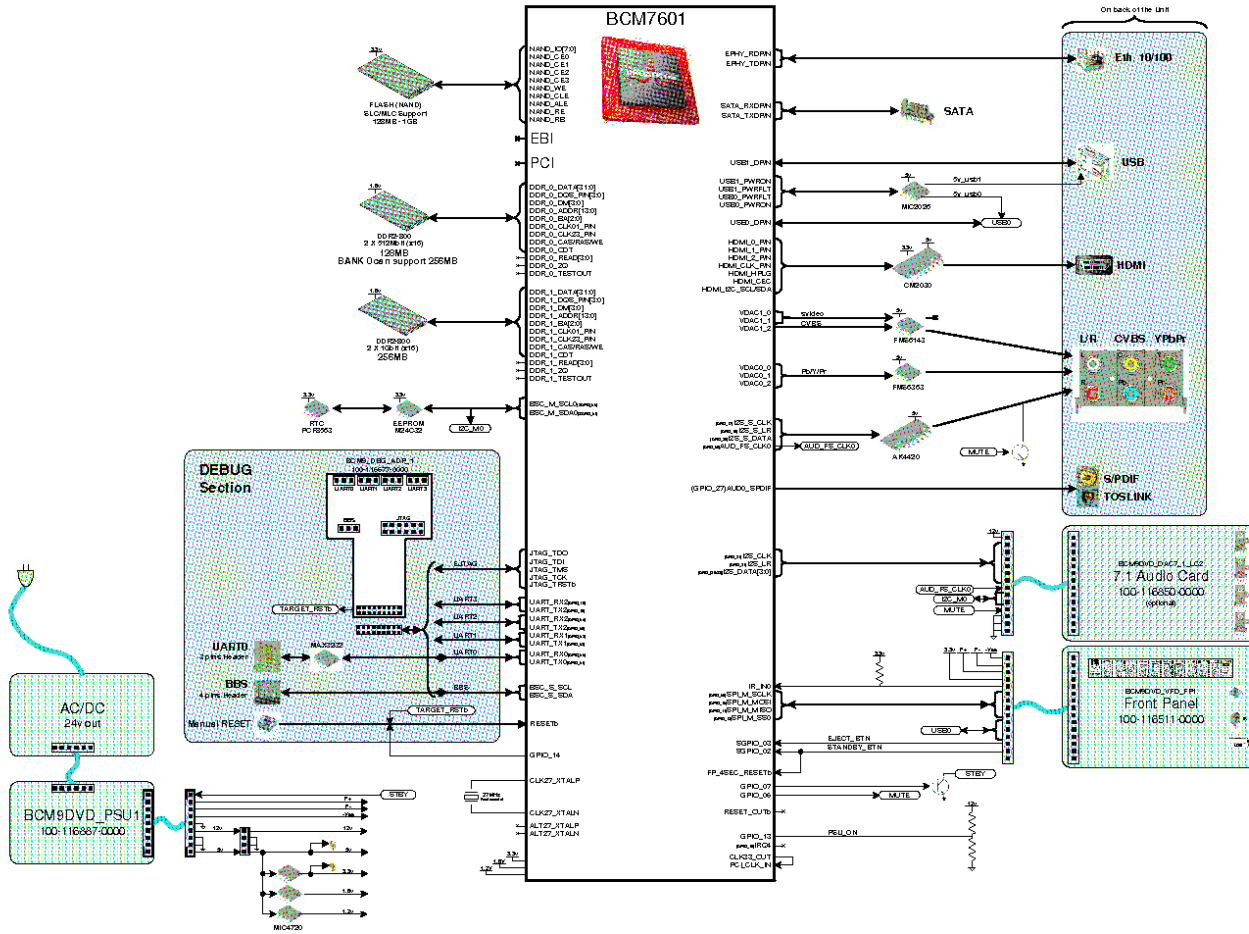


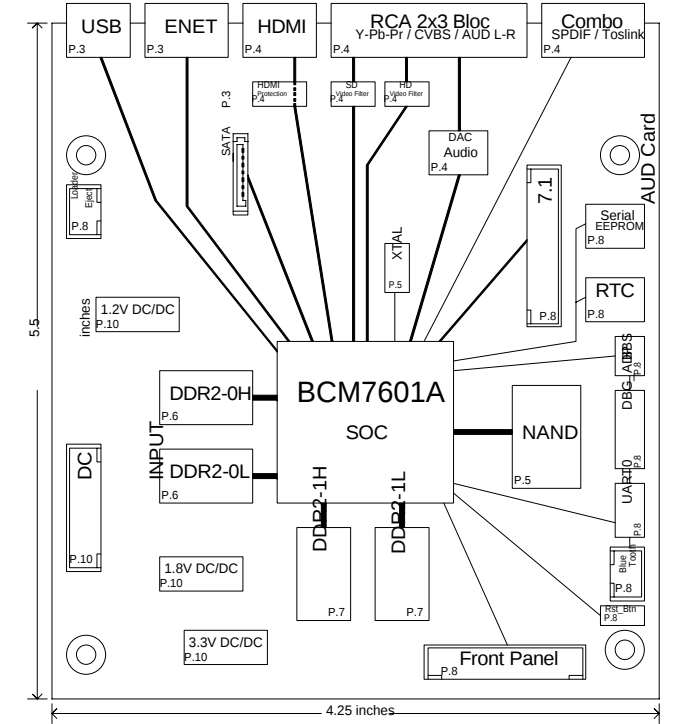
Block Diagram

BCM97601REF1A

2008-11-24

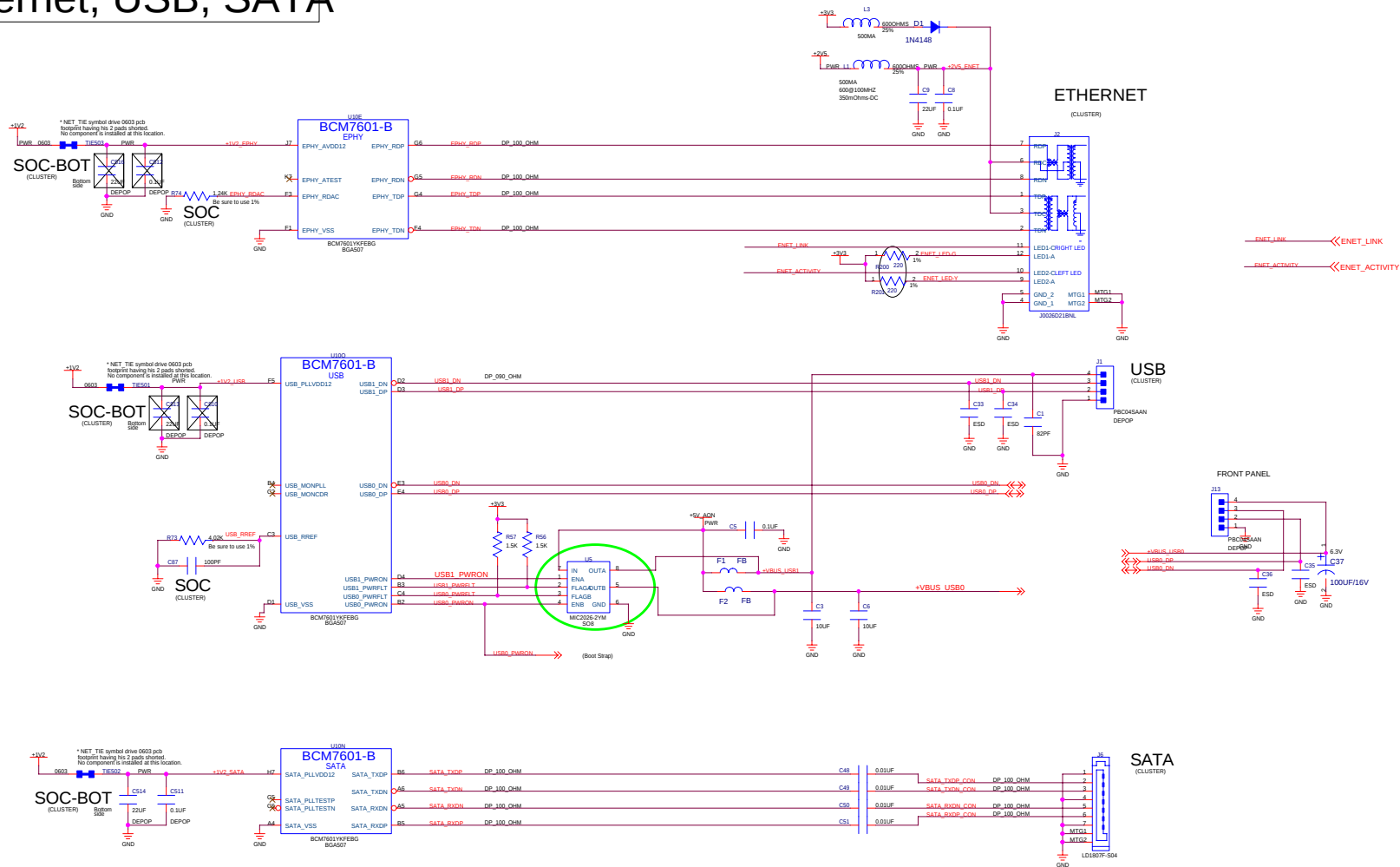


PCB LAYOUT / STACKUP OVERVIEW

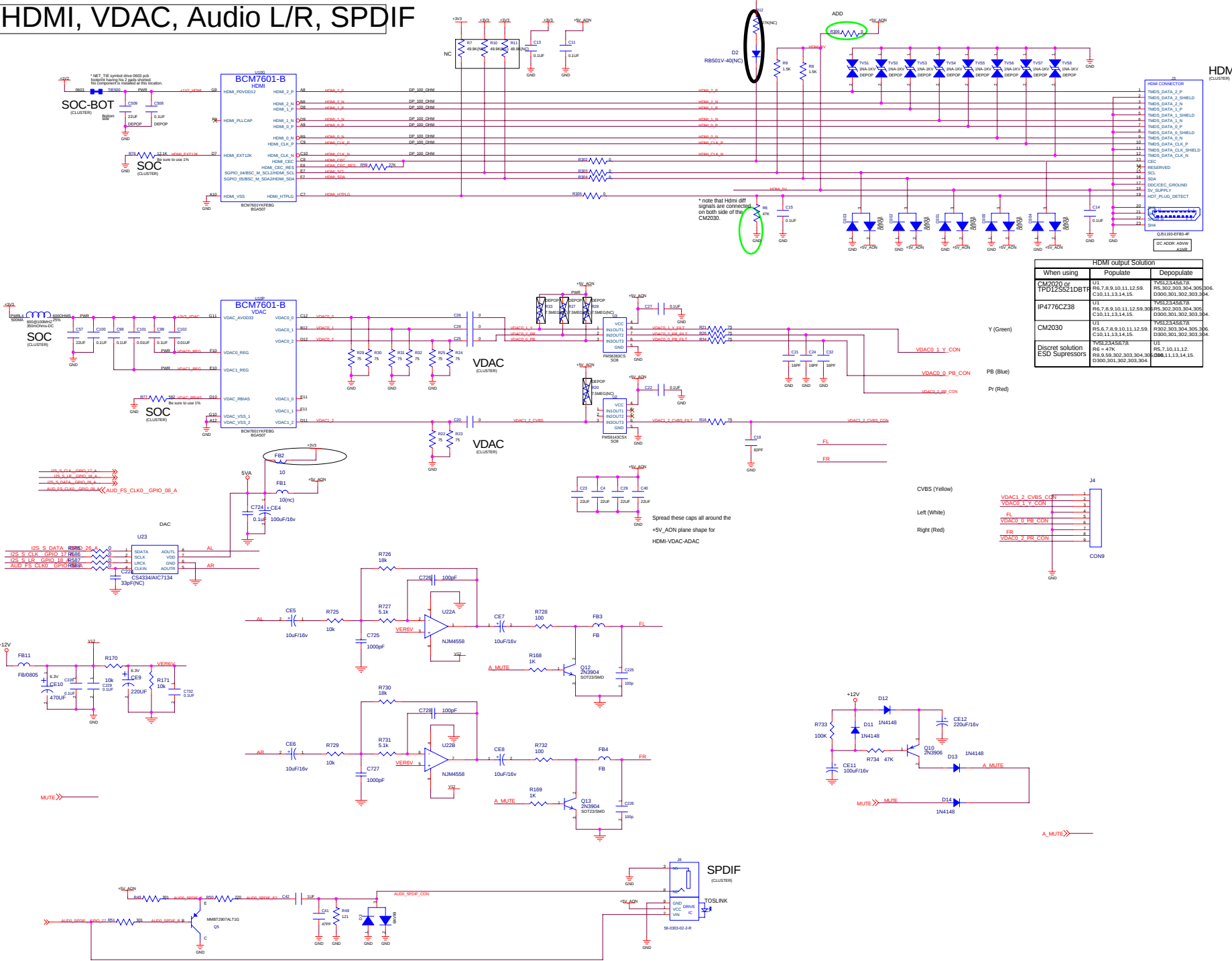


STACK-UP

Ethernet, USB, SATA



HDMI, VDAC, Audio L/R, SPDIF



HDMI output Solution		
When using	Populate	Depopulate
CM2030 or TP0125521DBTR	U1: R6.7, 8.9, 10, 11, 12, 59, C10, 11, 13, 14, 15.	Y6B12345678, R6, 302, 303, 304, 305, 306, C900, 301, 302, 303, 304.
IP4776C238	U1: R6.7, 8.9, 10, 11, 12, 59, 30, C10, 11, 13, 14, 15.	Y6B12345678, R6, 302, 303, 304, 305, C900, 301, 302, 303, 304.
CM2030	U1: R6.7, 8.9, 10, 11, 12, 59, C10, 11, 13, 14, 15.	Y6B12345678, R6, 302, 303, 304, 305, 306, C900, 301, 302, 303, 304.
Discret solution ESD Suppressors	Y6B12345678, R6 = 47K, R8, 9, 59, 302, 303, 304, 305, C10, 11, 13, 14, 15.	U1: R6.7, 10, 11, 12, 2, R6 = 47K, R8, 9, 59, 302, 303, 304.

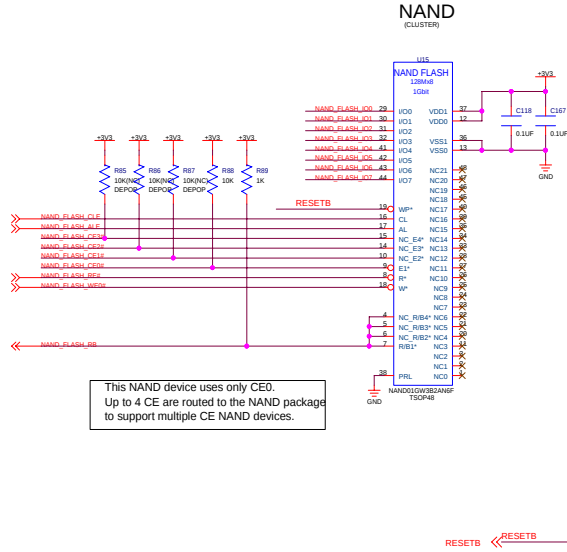
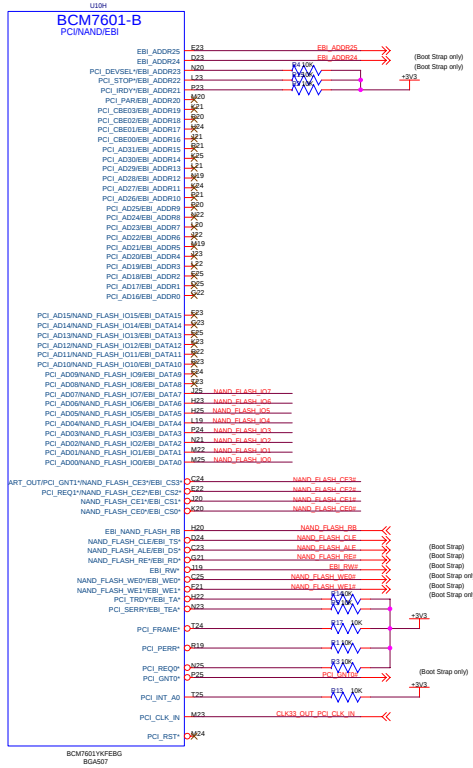
Y (Green)
PB (Blue)
Pr (Red)

CVBS (Yellow)
Left (White)
Right (Red)

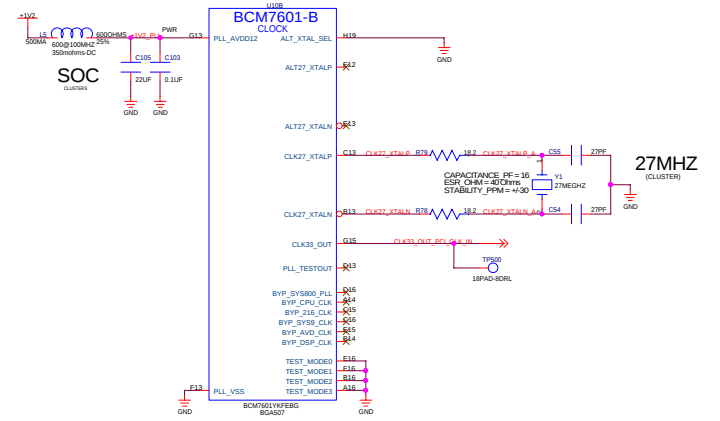
Spread these caps all around the
+5V_AGN plane shape for
HDMI-VDAC-ADAC

A_MUTE

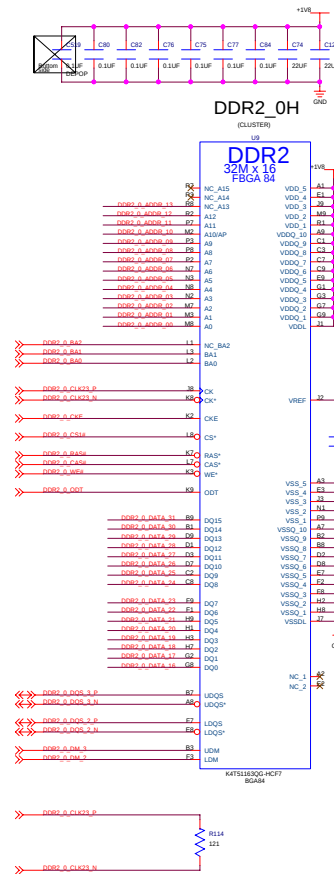
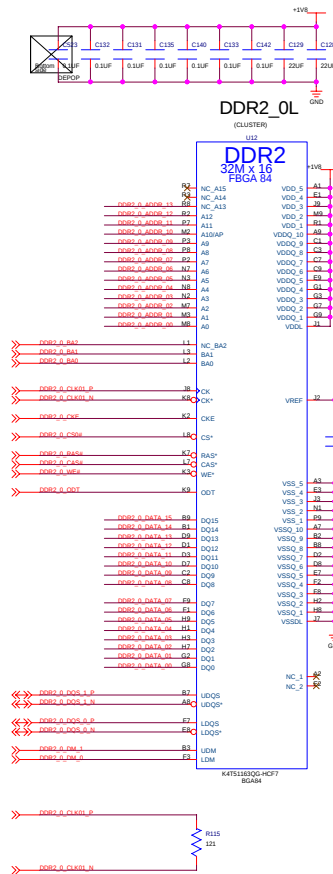
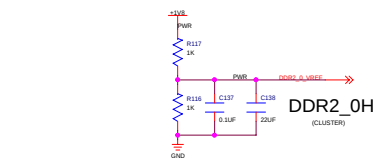
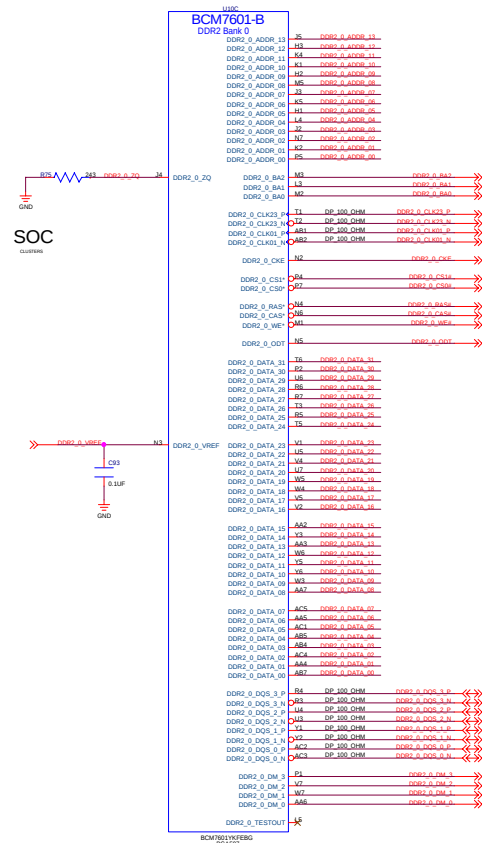
NAND



Clock



DDR2 Bank-0

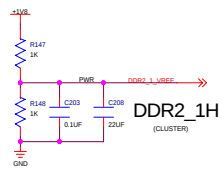
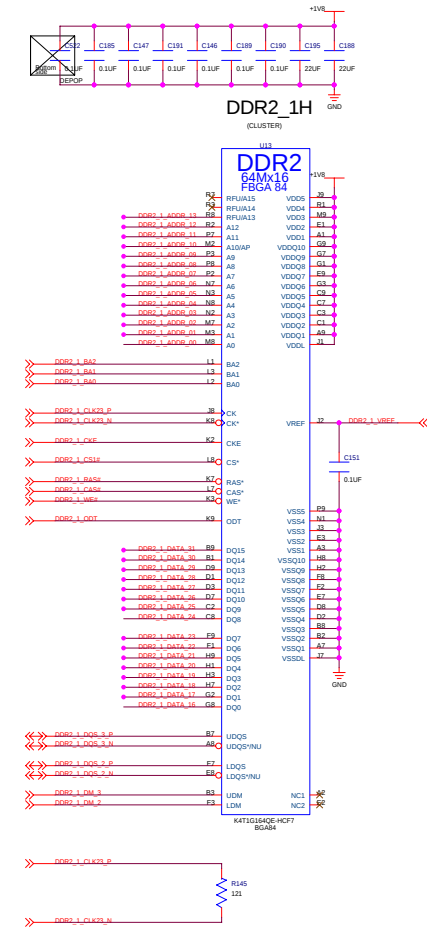
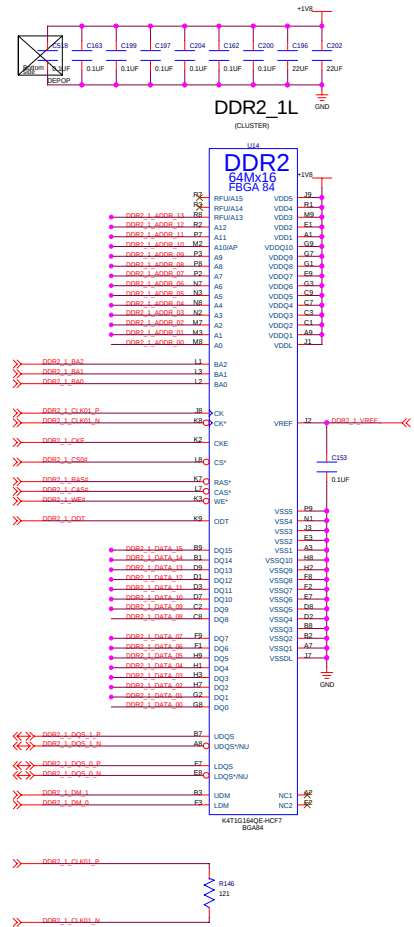
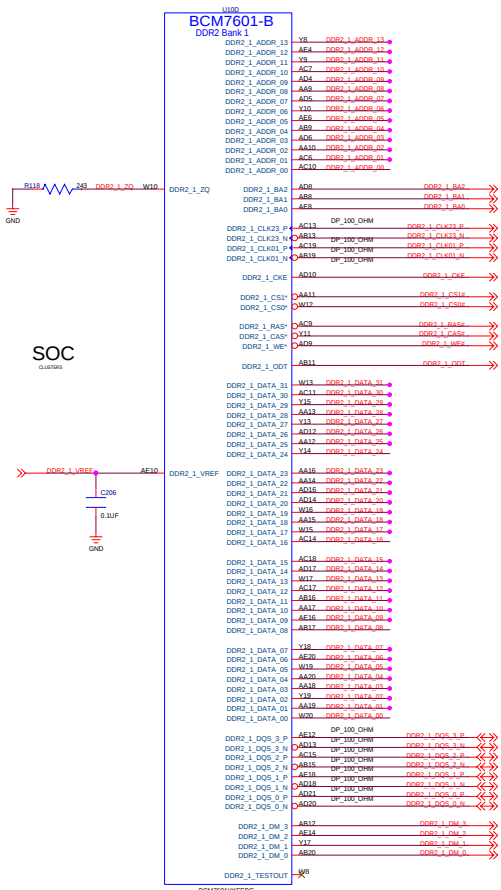


BCM7601 DDR2 2x16 --> Design notes and Layout Guidelines:

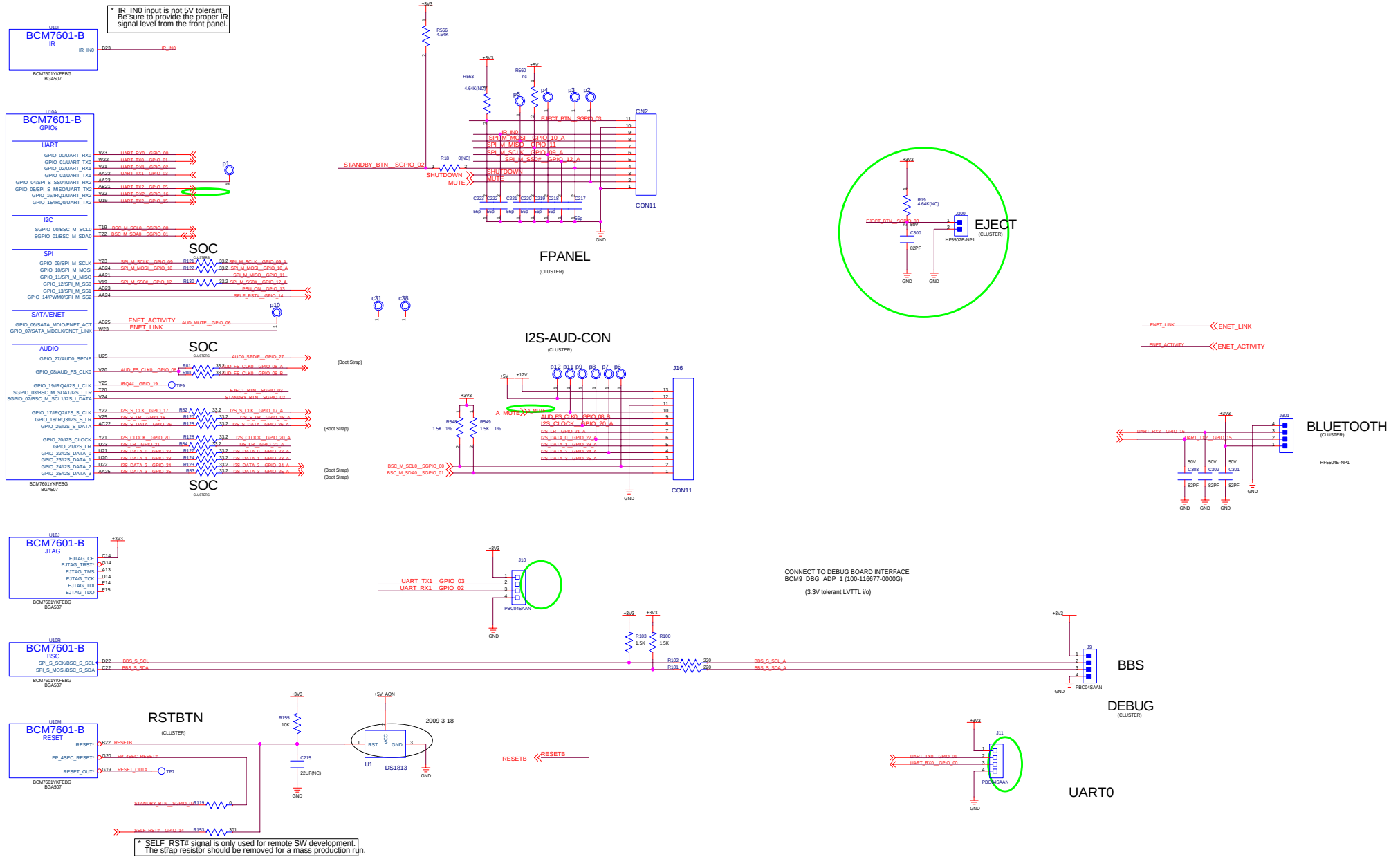
- 1- Length of all Data signals into a Byte Lane should be matched together (<300 mils).
- 2- Length of all Data signals between Byte Lane should be matched together (<550 mils).
- 3- DDR2 clock and DQS P/N traces must be routed as 100 Ohms Differential pairs. Traces width and gap according to PCB stackup.
- 4- When developing the PCB floor plan, the proximity of the DDR2 device to the memory controller is an important factor. If the memory is close to the controller, the layout is usually easier.
 - To avoid the use of external address termination on high-speed DDR2, the target address trace length should be 2.3in or less.
 - To avoid the use of external data termination on high-speed DDR2, the target data trace length should be 1.3in or less.

* If those requirements can not be reached, refer to JEDEC JESD79-2B standard for design rules and terminations.

DDR2 Bank-1

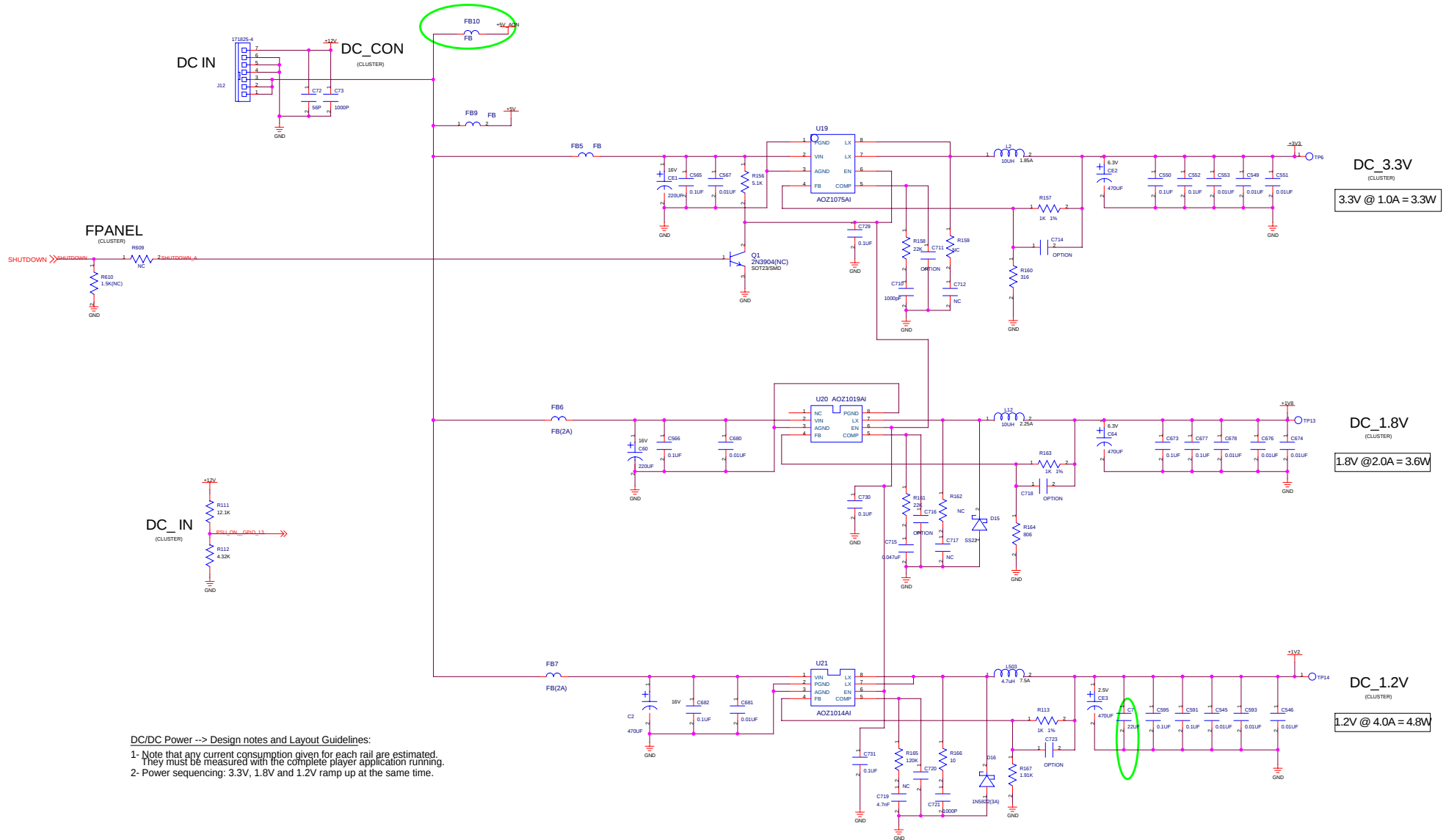


7.1 Card, FPanel, GPIOs, SPI, I2C, UART, BBS, JTAG, Reset, Debug-LED



DC/DC

PCB Mounting Holes:



BCM97601REF1A [P1]

824-117116-0000

BCM97601REF1A Reference Design

- 2
- 3
- 4
- 5
- 6
- 7
- 8
- 9
- 10
- Block Diagram
- Ethernet, USB, SATA
- HDMI, VDAC, Audio L/R, SPDIF
- NAND, Clock
- DDR2 Bank-0
- DDR2 Bank-1
- 7.1 Card, FPanel, GPIOs, SPI, I2C, UART, BBS, JTAG, Reset, Debug-LED
- Boot Strap Options, Core Power
- DC/DC

P1	2008-11-25	PR	BCG-04596	-	Initial Prototype Release.
					The list of change below shows the differences between a BCM97601REF1 assy# 100-116691-0000G and this new BCM97601REF1A ref design.
					* The REF1A has not been resequenced and use same refdes than the REF1 except for:
					* New resistors added are using refdes >= R300.
					* New capacitors added are using refdes >= C300.
					* New connectors added are using refdes >= J300.
					* New diodes added are using refdes >= D300.
					* The REF1A has no components populated on the bottom side.
2,3,4,5,6,7,8,9					- Replace BCM7601A0 chip by BCM7601B0 chip.
2					- Update diagram bloc with proper NAND and EEPROM density.
3,4					- Replace bottom resistor R500,501,502,503 by net-tie TIE500,501,502,503. Also depop bottom caps C508,510,511,512.
3					- Remove external RTerm. components R1,2,3,4 and C2,7.
4					- Replace SPDIF/TOSLINK J5 connector for new connector allowing the coaxial and the optical connection at the same time.
4					- Remove external audio mute circuitry (R40,42,43 and Q1,2,3,4 are removed).
4					- Remove audio DAC LPF components R36,37,39,44,46,47 and C35,38.
4					- Increase audio DAC power filtering. Replace L2 bead by 10 ohms R301 resistor. Replace C34 ceramic 22uF capacitor by electrolytic 470uF capacitor.
4					- DEPOP useless components R13,14,18,19 and C17,19 on the s-video lines.
4					- Correct CEC signal level issue; connect R12 CEC 27K PU to 3.3V instead of HDMI_5V.
4					- Modify HDMI output configuration to allow the using of ESD Suppressors if desired:
					+ Replace CM2030 by CM2020 and DEPOP R5.
					+ Add TVS1,2,3,4,5,6,7,8.
					+ Add R302,303,304,305,306 and D300,301,302,303,304.
5					- Replace 4Gbit SLC NAND by 1Gbit SLC NAND.
6,7					- On the DDR2_CLK lines, remove bottom side depop caps C517,520,524,525.
7					- Change DDR2 1Gbit from K4T1G164QQ-HCF7 to latest die rev K4T1G164QE-HCF7.
8					- Replace J14 front panel right angle pcb connector for a straight connector type.
8					- Add 10K PU resistor R300 on SPI_M_MISO_GPIO_11 signal.
8					- Add EJECT signal to loader J300 connector and capacitor C300.
8					- Add Bluetooth support J301 connector. Add C301,302,303.
8					- Replace U7 512Kbit EEPROM 5.28mm body package by 32Kbit 3.8mm body package.
8					- Remove AUD_FS_CLK0 buffering circuitry U11,C117 and R62. DEPOP capacitor C59.
8					- Remove R69 from the RTC circuit.
9					- Set strap_ebl_rom_size = 2 (4 bit NAND ECC enable). DEPOP R99, install R95.
9					- Remove bottom components C500,504,507,515. Was unused 1.2V decoupling caps.
10					- When possible, connect NC pins of 7601 to ground in order to help thermal dissipation.
10					- Replace C125 470uF capacitor by a small cap value of 82pF.
10					- Replace DC/DC switcher U17 and U18 MIC4720 by MIC4721.

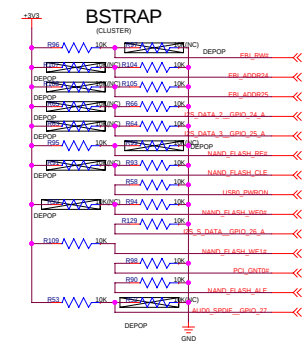
Boot Strap Options

SUN_TOP_CTRL.SUN_TOP_CTRL_STRAP_VALUE 0 = C0080481				
Field Name	Signal Name	Bit Field	Description	Force Default
1 strap_use_defaults	EBI_RW#	31	Forces usage of default values for strap signals 0 = All straps must be set on board 1 = Only non-default values need be set	N/A
1 strap_reset_outb_def_val	Internal (Hard Coded)	30	Default value of the reset_outb pin after hardware reset After hardware reset, the reset_outb pin will change to 1 (deasserted)	N/A
0 strap_test_debug_en_1	EBI_ADDR24	29	Test debug mode select	0
0 strap_test_debug_en_0	EBI_ADDR25	28	Security related (2 bits) *default = 0	0
0 Reserved	N/A	27	Reserved bit must be written with 0. A read returns an unknown value.	N/A
0 strap_33_27_mhz_clock	Internal (Hard Coded)	26	33 Mhz clock is used	N/A
0 Reserved	N/A	25	Reserved bit must be written with 0. A read returns an unknown value.	N/A
0 strap_xtal_sel	Refer to pin ALT_XTAL_SEL	24	XTAL select	N/A
0 strap_xtal_adj_3		23		N/A
0 strap_xtal_adj_2		22		N/A
0 strap_xtal_adj_1	I2S_DATA_2_GPIO_24_A	21	XTAL adjustment	0
0 strap_xtal_adj_0	I2S_DATA_3_GPIO_25_A	20	(This strap has no effect when using ALT_XTAL).	0
1 strap_ebi_rom_size_1	NAND_FLASH_RE#	19	NOR ROM (always 64 MB window): 0 = NOR flash 1 = OneNAND flash	N/A
0 strap_ebi_rom_size_0	NAND_FLASH_CLE	18	0 = Disable ECC 1 = 1 bit ECC 2 = reserved 3 = reserved	N/A
0 strap_ebi_invert_addr	USB0_PWRON	17	0 = Do not invert EBI address 1 = Invert upper bits of EBI address (Not used by NAND flash)	0
0 Reserved	N/A	16		N/A
0 Reserved	N/A	15	Reserved bit must be written with 0. A read returns an unknown value.	N/A
0 strap_pci_ext_arb	Internal (Hard Coded)	14	Internal Arb. (default)	N/A
0 strap_flash_width	NAND_FLASH_WE0#	13	NOR ROM: 0 = 8 bit 1 = 16 bit 1 = ignore write commands to block 0 (disallow writes)	N/A
0 strap_system_big_endian	I2S_S_DATA_GPIO_26_A	12	0 = Chip is operating as a little endian device in a big endian system 1 = Chip is operating as a big endian device in a big endian system	N/A
0 strap_ebi_cs_swap	Internal (Hard Coded)	11	0 = no swap 1 = swap cs_0 and cs_1	N/A
1 strap_nand_flash	NAND_FLASH_WE1#	10	0 = Boot from NOR 1 = Boot from NAND	N/A
0 strap_spi_slave_enable	PCI_GNT0#	9	0 = The Slave Serial Port (SSP) uses BSC protocol 1 = The SSP uses SPI protocol	0
0 strap_pci_memwin_size_1	Internal (Hard Coded)	8		N/A
1 strap_pci_memwin_size_0	Internal (Hard Coded)	7	1024 MB	N/A
0 strap_pci_memwin2_en	Internal (Hard Coded)	6	PCI memory window 2 is disabled	N/A
0 strap_pci_memwin1_en	Internal (Hard Coded)	5	PCI memory window 1 is enabled	N/A
0 strap_pci_client	NAND_FLASH_ALE	4	0 = Chip is a PCI master device 1 = Chip operates as a PCI slave device	0
0 Reserved	N/A	3		N/A
0 Reserved	N/A	2		N/A
0 Reserved	N/A	1	Reserved bit must be written with 0. A read returns an unknown value.	N/A
1 strap_reset_ext_mode	AUD0_SPDIF_GPIO_27	0	0 = reset_outb is not extended 1 = reset_outb is extended 200 ms	N/A

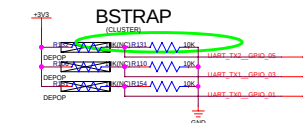
Boot strap option --> Design notes and Layout Guidelines:

1- Note these configuration resistors do not need to be close to the BCM7601. So, place them at the destination of the trace.

It will clear the BCM7601 area and help the fanout of the chip.



strap_use_defaults
strap_test_debug_en_1
strap_test_debug_en_0
strap_xtal_adj_1
strap_xtal_adj_0
strap_ebi_rom_size1
strap_ebi_rom_size0
strap_ebi_invert_addr
strap_flash_width
strap_system_big_endian
strap_nand_flash
strap_spi_slave_enable
strap_pci_client
strap_reset_ext_mode



Universal CFE version requires custom DDR2 boot strap configuration.

Core Power

